Attorney Docket No. 0756-1950

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2871
Shunpei YAMAZAKI et al.	)	Examiner: Minh Toan T. Ton
Serial No. 09/285,899	)	CERTIFICATE OF MAILING
Filed: April 9, 1999	)	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 10, 2006.
For: ELECTRO-OPTICAL DEVICE HAVING LEVELING FILM	)	
	)	

APPEAL BRIEF

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. § 134 and 37 C.F.R. § 1.192(a), the Appellant submits this Appeal Brief to appeal the examiner's final rejection of claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68 in the Official Action mailed August 9, 2005, and maintained in the *Advisory Action* mailed December 22, 2005, and further maintained in the Official Action April 10, 2006.

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I. REAL PARTY IN INTEREST

The named inventors have assigned all ownership rights in the pending application to Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036, Japan, which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

The appellant, their legal representatives, and the assignee are not aware of any other pending appeals or interferences which will directly affect or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 9-16, 21-24, 33-36, 50-52, 54 and 57-97 are pending in the present application, of which claims 9, 13, 21, 33, 57-59, 66, 69, 73, 77, 81, 85, 89 and 93 are independent. Claims 69-97 have been withdrawn from consideration (page 2, Paper No. 08042005). Accordingly, claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68 are currently elected, of which claims 9, 13, 21, 33, 57-59 and 66 are independent. No claims have been deemed allowable by the examiner.

IV. STATUS OF AMENDMENTS

All prior amendments are believed to have been entered in the present application. Thus, the status of the claims in this application is as set forth above and in Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a device, a television (e.g. Figure 9), a projector (e.g. Figure 17), or a portable computer (e.g. Figure 20), having at least one liquid crystal panel (e.g. Figures 7(A)-(I) and 12(A)-(E)), the liquid crystal panel comprising a first substrate (e.g. 50) having an insulating surface; a second substrate (e.g. 80) being opposed to the first substrate; at least one thin film transistor (TFT)/semiconductor element (e.g. 63 or 64) being formed over the first substrate, the TFT/semiconductor element including at least a channel region, source and drain regions (e.g. 55, 56 or 59, 60) with the channel region therebetween, a gate insulating film (e.g. 65) adjacent to the

channel region and a gate electrode (e.g. 66 or 67) adjacent to the channel region with the gate insulating film interposed therebetween; where the channel region, the source and drain region of the one TFT/semiconductor element is formed in a semiconductor island; an organic resin/leveling film (e.g. 77) formed over the first substrate to provide a leveled upper surface over the first substrate, the organic resin/leveling film covering the TFT/semiconductor element; a pixel electrode (e.g. 71) formed on the leveled upper surface, the pixel electrode being electrically connected to the TFT/semiconductor element through an opening (e.g. Figure 7(H); page 14, lines 28-29; formed by mask P7) formed in the organic resin/leveling film; a liquid crystal material having ferroelectricity or antiferroelectricity (e.g. page 36, lines 2-6) and being formed between the first substrate and the second substrate; and an opposed electrode (e.g. 90) formed over the second substrate and opposed to the pixel electrode with the liquid crystal material interposed therebetween. When the device is a television (e.g. Figure 9), the television further comprises a tuner (e.g. 223) for receiving television radio waves; and the liquid crystal panel is operationally connected to the tuner.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Request for consideration of outstanding Information Disclosure Statements.

B. Whether claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68 are not *prima facie* obvious based on the combination of U.S. Patent No. 5,227,900 to Inaba et al., Japanese Patent Application Publication No. 61-141174 to Takeshita et al., and U.S. Patent No. 5,055,899 to Wakai et al. The rejected claims shall stand or fall together.

VII. ARGUMENTS

A. Request for consideration of outstanding Information Disclosure Statements.

As noted in detail below, the Appellant has made at least three previous requests for complete consideration of the Information Disclosure Statement filed December 3,

1999. It is respectfully requested that the Examiner attend to these matters before forwarding the present application to the Board.

Specifically, the Appellant notes the *partial* consideration of the IDS filed on December 3, 1999 (received by OIPE December 7, 1999). Specifically, despite three previous requests, it appears that the Examiner continues to overlook the citation of JP 58-158967 on Form PTO-1449 filed with the IDS filed December 3, 1999. The partially considered 1449, which was attached to Paper No. 18 (mailed December 13, 2000), does not appear in the Image File Wrapper (IFW); however, the partially considered 1449 was attached to the copy of the Official Action mailed to the Appellant. Also, the Appellant attached a copy of the partially considered 1449 to the *Amendment* filed January 10, 2005 (received January 12, 2005); however, the IFW does not include a copy of this submission. Apparently, these documents were not included in the scanning process. As a courtesy to the Examiner, the Appellant attached a copy of the partially considered Form PTO-1449 with the *After Final Response* filed December 9, 2005 (see IFW under the listing "12/12/2005 Information Disclosure Statement (IDS) Filed PROSECUTION," page 3). It is noted that the Appellant resubmitted the Form PTO-1449 as a courtesy to the Examiner. It is respectfully submitted that the above-referenced IDS was properly filed on December 3, 1999, and should be accorded its filing date for the purposes of consideration and compliance with 37 CFR 1.97 and 1.98. The Appellant respectfully requests that the Examiner provide an initialed copy of the Form PTO-1449 evidencing consideration of JP '967.

B. Whether claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68 are not *prima facie* obvious based on the combination of U.S. Patent No. 5,227,900 to Inaba et al., Japanese Patent Application Publication No. 61-141174 to Takeshita et al., and U.S. Patent No. 5,055,899 to Wakai et al.

The Official Action continues to reject claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68 as obvious based on the combination of U.S. Patent No. 5,227,900 to Inaba et al., Japanese Patent Application Publication No. 61-141174 to Takeshita et al., and U.S. Patent No. 5,055,899 to Wakai et al. The Appellant respectfully traverses the rejection because the Official Action has not made a *prima facie* case of obviousness.

Initially, it is noted that the arguments with respect to a lack of motivation to combine Inaba and Takeshita were originally presented in an *Appeal Brief* filed June 7, 2004. In response to the *Appeal Brief*, prosecution was reopened in order to introduce Wakai. However, for the reasons noted in detail below, the Appellant respectfully submits that Wakai does not cure the deficiencies in the alleged motivation to combine Inaba and Takeshita. The Official Action mailed April 20, 2005, restricted claims 69-97 as a separate species. In response, the Appellant elected claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68. A final Official Action was mailed August 9, 2005, and the Appellant responded in detail in the *After Final Response* mailed December 9, 2005. An Advisory Action was issued December 22, 2005, without further comment. The Appellant filed a Request for Continued Examination in order to submit an Information Disclosure Statement on March 9, 2006. The final Official Action mailed April 10, 2006 (Paper No. 03312006), essentially duplicates arguments made by the Examiner in the Official Action mailed August 9, 2005 (Paper No. 08042005).

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

As noted in MPEP § 2142, the initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). It is respectfully submitted that Inaba and Takeshita fail to expressly or impliedly suggest all the features of the independent claims of the present invention. It is further submitted that the Examiner has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

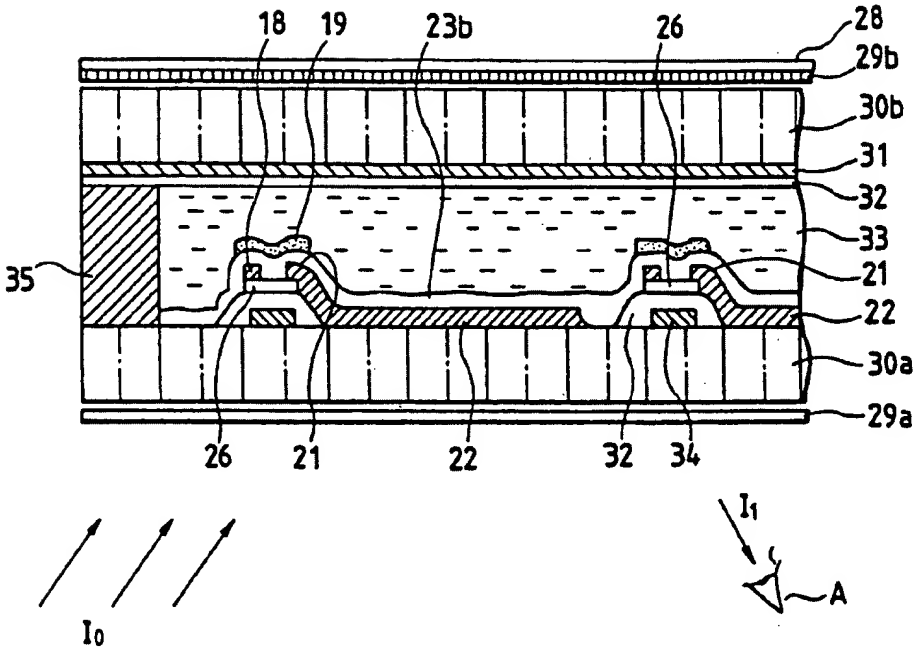
Further, it should be noted that the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680 (Fed. Cir. 1990). In other words, simply because the references can be combined does not mean that they should be combined. Thus, simply because one could combine and modify the teachings of Inaba, Takeshita and Wakai, does not mean one of skill in the art would do so absent some suggestion of the desirability of doing so. As noted in detail below, the Official Action has not demonstrated why one would have necessarily modified Inaba, Takeshita and Wakai in the manner suggested in the Official Action and in order to achieve the features of the claims of the present application.

There is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Inaba and Takeshita or to combine reference teachings to achieve the claimed invention. The present invention is directed to a liquid crystal panel (e.g. Figures 7(A)-(I) and 12(A)-(E)) comprising an organic resin/leveling film (e.g. 77) formed over a first substrate (e.g. 50) to provide a leveled upper surface over the first substrate, the organic resin/leveling film covering a TFT/semiconductor element (e.g. 63); and a pixel electrode (e.g. 71) formed on the leveled upper surface, the pixel electrode being electrically connected to the TFT/semiconductor element through an opening (e.g. Figure 7(H); page 14, lines 28-29;

formed by mask P7) formed in the organic resin/leveling film. The prior art does not contain sufficient motivation to teach or suggest to one of ordinary skill in the art at the time of the invention that it would have been obvious to combine Inaba and Takeshita in order to form a liquid crystal panel comprising an organic resin/leveling film formed over a first substrate to provide a leveled upper surface over the first substrate, the organic resin/leveling film covering a TFT/semiconductor element; and a pixel electrode formed on the leveled upper surface, the pixel electrode being electrically connected to the TFT/semiconductor element through an opening formed in the organic resin/leveling film.

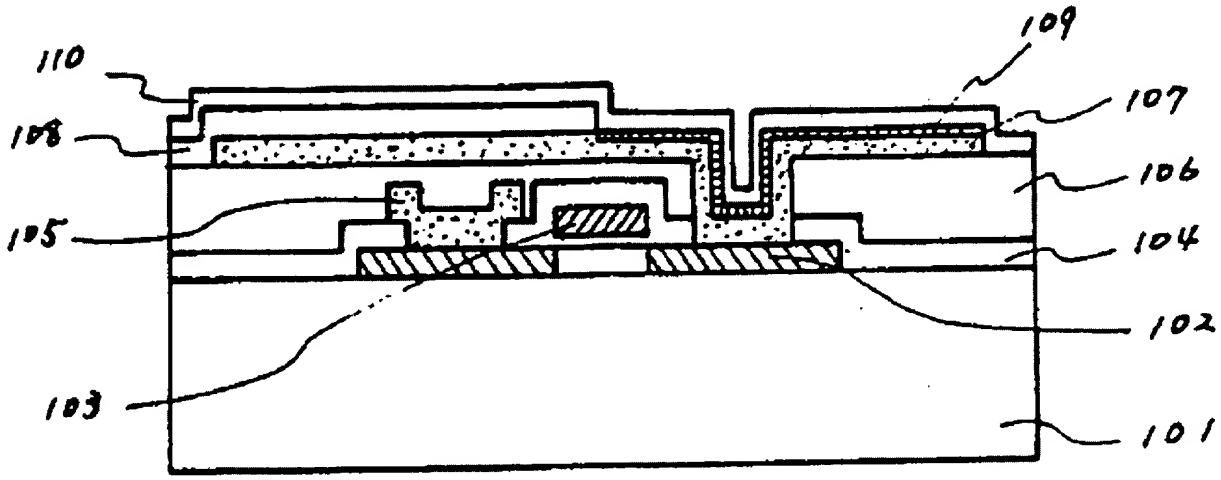
Inaba (Figure 5, reproduced below) appears to teach a substrate 30a, a gate electrode 34 on the substrate 30a, an insulating film 32 on the gate electrode 34, a semiconductor film 26 on the insulating film 32, a source 18 and a drain 21 of a TFT on the semiconductor film 26, a pixel electrode 22 in the same layer as the drain 21 of the TFT, and an insulating layer 23b covering all the features noted above. The Official Action concedes that Inaba does not teach "the organic resin film leveling layer and the pixel electrode formed on top of the leveling layer" (page 2, Paper No. 21). The Appellant further submits that Inaba does not teach or suggest an organic resin/leveling film formed over a first substrate 30a to provide a leveled upper surface over the first substrate, the organic resin/leveling film covering a TFT/semiconductor element 18, 21, 26, 32 and 34. Although Inaba teaches a pixel electrode 22, Inaba does not teach or suggest that the pixel electrode 22 be formed on a leveled upper surface, or that the pixel electrode is electrically connected to the TFT/semiconductor element 18, 21, 26, 32 and 34 through an opening formed in the organic resin/leveling film.

FIG. 5



The Appellant respectfully submits that in order to render obvious the present invention, it appears that the Official Action would have to somehow find motivation to separate pixel electrode 22 from drain 21, to insert an organic resin/leveling film between the TFT 18, 21, 26, 32 and 34 and the pixel electrode 22 which covers the TFT 18, 21, 26, 32 and 34, to form an opening in the organic resin/leveling film, and to connect the pixel electrode 22 to the TFT 18, 21, 26, 32 and 34 through the opening. For reasons noted in detail below, Takeshita and Wakai do not contain sufficient motivation for all of the steps required to convert the device of Inaba into a device which renders obvious the present invention.

Takeshita (Figure 1(a), reproduced below) appears to teach a solid state image pickup device comprising an insulating substrate 101, a nondoped polycrystalline silicon layer 102 and an interlayer insulating film 104 on the substrate 101, a gate electrode 103 in the interlayer insulating film 104 and over the silicon layer 102, a polyimide resin 106 on the interlayer insulating film 104, a contact hole in the interlayer insulating film 104 and the polyimide resin 106, and a conductive thin film 107 formed in the contact hole and apparently in contact with the nondoped polycrystalline silicon layer 102.



(a)

The Official Action asserts that Takeshita teaches "that the usual way of forming a TFT is by forming a leveling layer" (page 2, Paper No. 21). This is a mischaracterization of Takeshita. Rather, Takeshita states that "[u]sually, poly-silicon TFTs are formed by the above mentioned method" (page 3, translation of Takeshita). The Appellant respectfully submits that Takeshita is directed to a solid state image pickup device, which comprises TFTs, and that TFTs for a solid state image pickup device include a polyimide resin 106 "for leveling as an interlayer insulating film" (Id.). Just because Takeshita states that TFTs are usually formed by a method which includes a polyimide resin 106, this certainly does not in and of itself teach how or why a polyimide resin 106 would be incorporated into the Inaba device, which is a method of driving a ferroelectric liquid crystal element. Specifically, the mere teaching of a polyimide resin 106 in Takeshita does not teach one of ordinary skill in the art at the time of the invention to modify the Inaba device by separating pixel electrode 22 from drain 21, inserting the polyimide resin 106 of Takeshita between the TFT 18, 21, 26, 32 and 34 and the pixel electrode 22 which covers the TFT 18, 21, 26, 32 and 34, to form an opening in the organic resin/leveling film, and connecting the pixel electrode 22 to the TFT 18, 21, 26, 32 and 34 through the opening.

Also, it is noted that Inaba is a fully functional device. The statement in Takeshita that "usually, poly-silicon TFTs are formed by the above mentioned method" does not provide one of ordinary skill in the art with sufficient motivation to modify the fully

functional Inaba device, particularly absent any disclosure or suggestion of any advantage to be achieved by such modification. It is respectfully submitted that the broad assertion that TFTs are "usually" formed in this fashion completely fails to provide a convincing line of reasoning as to why one of ordinary skill in the art would have been motivated to modify Inaba as proposed.

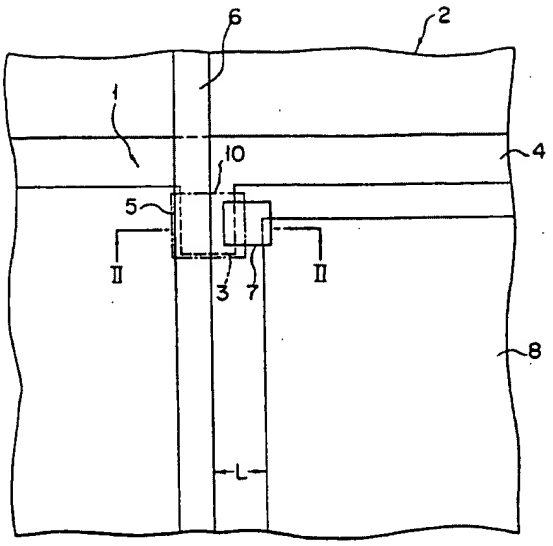
Further, Inaba was published in 1993 and Takeshita was published in 1986. Clearly, Inaba et al. were aware of the teachings of Takeshita et al. in 1993. If it were important to Inaba et al. to have a leveling layer in a liquid crystal device, particularly one formed between a TFT and a pixel electrode, then why is Inaba silent as to the importance of such feature? The Appellant respectfully submits that no such teaching is provided in Inaba, because it was not obvious at the time of the invention that it would have been desirable to provide a liquid crystal panel with a leveling layer formed between a TFT and a pixel electrode of the liquid crystal panel.

The Official Action further asserts that "it would have been obvious ... to combine the leveling layer of Takeshita et al with the ferroelectric display of Inaba et al since, as taught by Inaba et al, this was well known" (Id.). Specifically, it appears that the Official Action is asserting that combining the leveling layer of Takeshita with the ferroelectric display of Inaba was well known. Nothing in the prior art supports this assertion. The Official Action has not provided any specific teaching from either Inaba or Takeshita to indicate how or why one would of ordinary skill would have been motivated to combine the teachings of Inaba and Takeshita. Specifically, it is not clear how or why one might separate the pixel electrode 22 and the drain 21 of Inaba, insert the polyimide resin 106 of Takeshita between the TFT 18, 21, 26, 32 and 34 and the pixel electrode 22 of Inaba, form an opening as taught in Takeshita in the proposed combined device, and connect the pixel electrode 22 of Inaba to the TFT 18, 21, 26, 32 and 34 via the opening of Takeshita. In Inaba, it appears that the source 18, drain 21 and pixel electrode 22 are formed in the same layer. It is not clear from Takeshita why one of ordinary skill in the art would have been motivated to divide this layer of Inaba, much less add the additional components from the Takeshita device to the Inaba device. The Official Action relies on a broad assertion that this is all "well known" without providing any specific teaching to support the assertion.

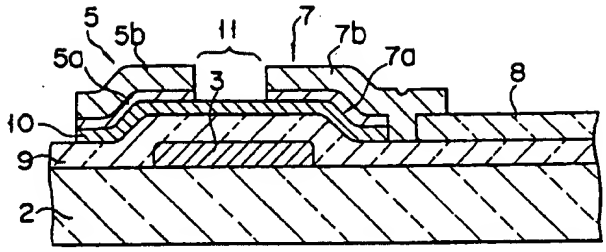
Also, as noted in the Appellant's *Amendment* filed March 13, 2001, and again in the Appellant's *After Final Amendment* filed October 5, 2001, Inaba and Takeshita fail to appreciate the problem caused by the narrow cell gap of the ferroelectric liquid crystal (FLC) or anti-ferroelectric liquid crystal (AFLC) display device, and the materiality of the flatness of the inside surface of the substrate in the FLC/AFLC display. The Official Action responded to these arguments only by stating that limitations from the specification are not read into the claims (page 2, Paper No. 26). This misses the point. As noted above, the organic resin film or leveling film of the independent claims of the present invention is formed over the first substrate in order to provide a leveled upper surface over the first substrate. Inaba does not discuss the problem caused by the narrow cell gap, and the materiality of the flatness of the inside surface of the substrate in the FLC/AFLC display, and, as noted above, there is no motivation in Inaba or Takeshita to modify the Inaba device to include such a feature. Reconsideration of the rejection of the independent claims is respectfully requested.

Wakai does not cure the deficiencies in the alleged motivation to combine Inaba and Takeshita. Specifically, Wakai does not teach or suggest why one would have been motivated to incorporate either polyimide resin 106 of Takeshita or insulating film 108 of Wakai into the Inaba device.

The Official Action begins by noting "a short-circuiting between the pixel electrode and the drain electrode" (page 2, Paper No. 08042005) and cites column 2, lines 18-27 and 63-68 of Wakai, which is a discussion the TFT shown Figures 1 and 2 (reproduced below). This portion of Wakai discusses concerns over short-circuiting "between transparent electrode 8 and drain line 6" (column 2, lines 24-25) (column 2, lines 61-62).



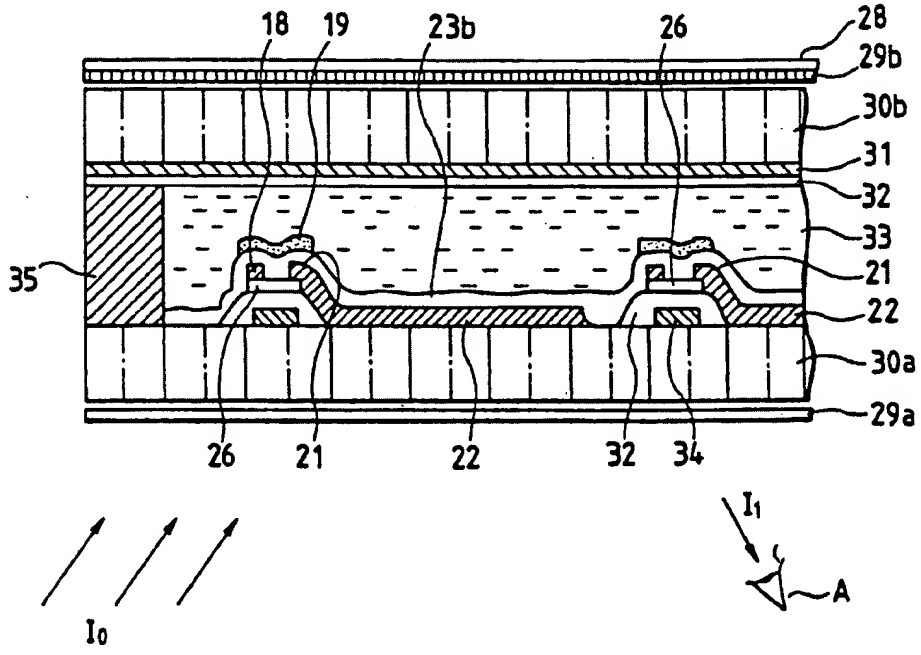
F I G. 1 (PRIOR ART)



F I G. 2 (PRIOR ART)

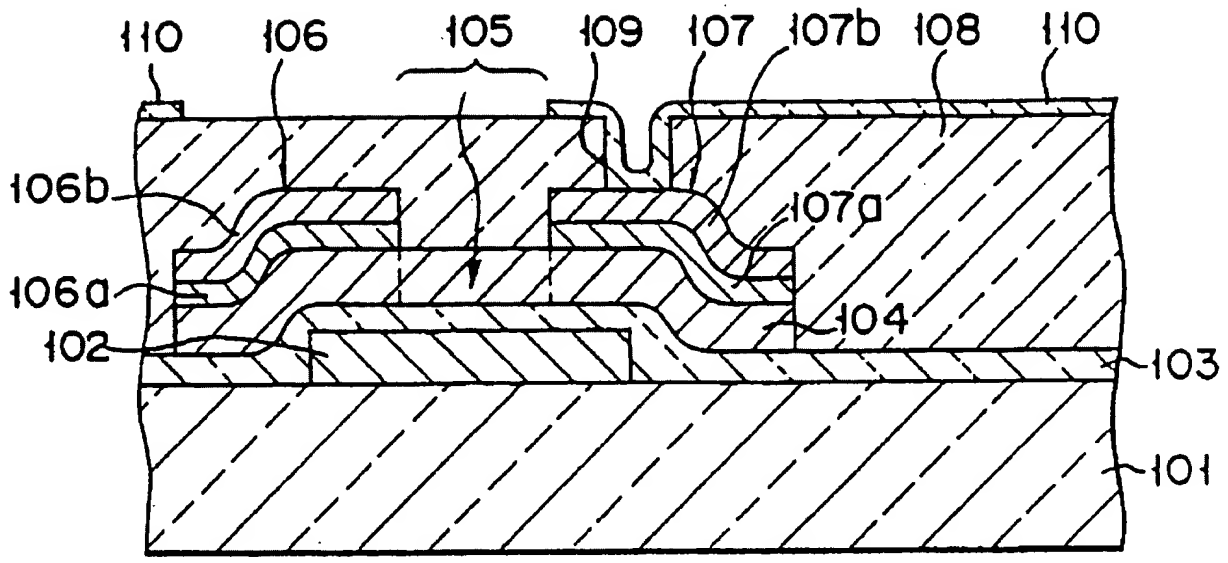
Then, the Official Action asserts that "Inaba discloses this similar conventional structure of having the pixel electrode directly connected to the drain electrode" (Id.). That is, the Official Action appears to be asserting that the TFT shown in Figures 1 and 2 of Wakai is similar to the TFT shown in Figure 5 of Inaba (reproduced below).

FIG. 5



The Official Action implies that the TFT of Figure 5 of Inaba would have a short-circuiting problem similar to that discussed in Figures 1 and 2 of Wakai. However, it is not clear that Inaba would have a short-circuiting problem similar to Wakai. In Inaba, for example, insulating layer 23b is provided between pixel electrode 22 and TFT terminal (source) 18. Also, in Figures 1 and 2 of Wakai (reproduced above), short-circuiting tends to occur between the transparent electrode (pixel electrode) 8 and the drain line 6 (column 6, lines 24-25). The Appellant notes that the pixel electrode 8 and the drain line 6 are separated from each other, and that short-circuiting tends to occur due to relatively short distance L (Figure 1; column 2, lines 26-39). Referring to Figure 5 of Inaba (reproduced above), the pixel electrode 22 is connected to the terminal 21 (source or drain electrode). However, Inaba fails to disclose a location of a line connected to the other terminal 18. Furthermore, Inaba fails to teach or suggest a distance between the pixel electrode 22 and a hypothetical line connected to the other terminal 18. The short-circuiting problem of Wakai would not have been applied to Inaba, because Inaba does not show a line connected to terminal 18. That is, nothing in the prior art or in the disclosure of Inaba teaches or suggests that short-circuiting was a problem for the device illustrated, for example, in Figure 5 of Inaba. Therefore, the Official Action has not shown why one of ordinary skill in the art at the time of the invention would have assumed a short-circuiting problem in Inaba and furthermore been led to completely reconfigure and redesign Inaba in a manner similar to that proposed in Wakai. As such, it is not clear why one would have been motivated to apply the teachings of Wakai to Inaba and/or Takeshita.

The Official Action further asserts that "Wakai solves the short-circuiting problem by forming the insulation/leveling layer ... between the pixel electrode and the drain electrode" and that "it would have been obvious to one of ordinary skill in the art to employ an insulating/leveling layer ... for avoiding disadvantages including short-circuiting" (pages 2-3, Id.). The Official Action, although not specific, appears to be referring to the insulating film 108 of Wakai, illustrated in Figure 3 (reproduced below).



The Official Action appears to assert that Wakai's discussion of a short-circuiting problem cures all the deficiencies in Inaba and Takeshita. The Appellant respectfully disagree and traverse the above-referenced assertions in the Official Action.

Wakai discloses that the formation of insulating film 108 decreases "the probability of short-circuiting between the drain and source electrodes 106 and 110" (column 15, lines 17-18). However, Wakai does not teach or suggest that insulating film 108 has anything to do with leveling. In other words, there is no nexus between insulating film 108 of Wakai and leveling. The Official Action does not explain why one of ordinary skill in the art would have looked to Wakai, which discusses short-circuiting, in order to form a leveling film.

Also, the disclosure of Wakai does nothing further to teach or suggest that one of ordinary skill in the art at the time of the present invention would have been motivated to separate pixel electrode 22 from drain 21 of Inaba, insert an organic resin/leveling film (in theory, either polyimide resin 106 of Takeshita or insulating film 108 of Wakai) between the TFT 18, 21, 26, 32 and 34 and the pixel electrode 22 which covers the TFT 18, 21, 26, 32 and 34, form an opening in the organic resin/leveling film, and connect the pixel electrode 22 to the TFT 18, 21, 26, 32 and 34 through the opening.

Therefore, the Appellant respectfully submits that the Official Action has not provided a proper suggestion or motivation, either in the references themselves or in

the knowledge generally available to one of ordinary skill in the art, to modify Inaba, Takeshita and Wakai or to combine reference teachings to achieve the claimed invention.

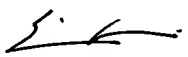
In the present application, it is respectfully submitted that the prior art of record, either alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

For all of the above reasons, it is respectfully asserted that the pending claims of the present application are unobvious in view of the prior art of record. Reversal of the outstanding rejections of record and allowance of the claims of this application is requested.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789

VIII. APPENDICES

APPENDIX A

PENDING CLAIMS

1.-8. (Canceled)

9. (Previously Presented) A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

10. (Original) A device according to claim 9, wherein said organic resin film comprises polyimide.

11. (Original) A device according to claim 9, wherein said pixel electrode is transparent.

12. (Original) A device according to claim 9, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

13. (Previously Presented) A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one semiconductor element being formed over the first substrate, said semiconductor element including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one semiconductor element is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said semiconductor element;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said semiconductor element through an opening formed in said organic resin film;

a liquid crystal material having ferroelectricity and being formed between the first substrate and the second substrate, and

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

14. (Previously Presented) A device according to claim 13, wherein said organic resin film comprises polyimide.

15. (Previously Presented) A device according to claim 13, wherein said pixel electrode is transparent.

16. (Previously Presented) A device according to claim 13, wherein said semiconductor element is a top-gate type thin film transistor in which said gate electrode is located above said channel region.

17.-20. (Canceled)

21. (Previously Presented) A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

22. (Original) A television according to claim 21, wherein said organic resin film comprises polyimide.

23. (Original) A television according to claim 21, wherein said pixel electrode is transparent.

24. (Original) A television according to claim 21, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

25.-32. (Canceled)

33. (Previously Presented) A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

34. (Original) A portable computer according to claim 33, wherein said organic resin film comprises polyimide.

35. (Original) A portable computer according to claim 33, wherein said pixel electrode is transparent.

36. (Original) A portable computer according to claim 33, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

37.-49. (Canceled)

50. (Previously Presented) A device according to claim 9, wherein the semiconductor island is a crystalline semiconductor island.

51. (Previously Presented) A device according to claim 13, wherein the semiconductor island is a crystalline semiconductor island.

52. (Previously Presented) A television according to claim 21, wherein the semiconductor island is a crystalline semiconductor island.

53. (Canceled)

54. (Previously Presented) A portable computer according to claim 33, wherein the semiconductor island is a crystalline semiconductor island.

55.-56. (Canceled)

57. (Previously Presented) A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and

a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain region of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

58. (Previously Presented) A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and

a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

59. (Previously Presented) A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

60. (Previously Presented) A device according to claim 57, wherein said semiconductor island is a crystalline semiconductor island.

61. (Previously Presented) A device according to claim 57, wherein said pixel electrode is transparent.

62. (Previously Presented) A television according to claim 58, wherein said semiconductor island is a crystalline semiconductor island.

63. (Previously Presented) A television according to claim 58, wherein said pixel electrode is transparent.

64. (Previously Presented) A portable computer according to claim 59, wherein said semiconductor island is a crystalline semiconductor island.

65. (Previously Presented) A portable computer according to claim 59, wherein said pixel electrode is transparent.

66. (Previously Presented) A projector having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

67. (Previously Presented) A projector according to claim 66, wherein said semiconductor island is a crystalline semiconductor island.

68. (Previously Presented) A projector according to claim 66, wherein said pixel electrode is transparent.

69. (Withdrawn, Previously Presented) A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having anti-ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

70. (Withdrawn, Previously Presented) A device according to claim 69, wherein said organic resin film comprises polyimide.

71. (Withdrawn, Previously Presented) A device according to claim 69, wherein said pixel electrode is transparent.

72. (Withdrawn, Previously Presented) A device according to claim 69, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

73. (Withdrawn, Previously Presented) A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having anti-ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

74. (Withdrawn, Previously Presented) A television according to claim 73, wherein said organic resin film comprises polyimide.

75. (Withdrawn, Previously Presented) A television according to claim 73, wherein said pixel electrode is transparent.

76. (Withdrawn, Previously Presented) A television according to claim 73, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

77. (Withdrawn, Previously Presented) A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate being opposed to the first substrate;

at least one thin film transistor being formed over the first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein the channel region, the source and drain region of said one thin film transistor is formed in a semiconductor island;

an organic resin film formed over said first substrate to provide a leveled upper surface over said first substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a liquid crystal material having anti-ferroelectricity and being formed between the first substrate and the second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

78. (Withdrawn, Previously Presented) A portable computer according to claim 77, wherein said organic resin film comprises polyimide.

79. (Withdrawn, Previously Presented) A portable computer according to claim 77, wherein said pixel electrode is transparent.

80. (Withdrawn, Previously Presented) A portable computer according to claim 77, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

81. (Withdrawn, Previously Presented) A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain region of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having anti-ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

82. (Withdrawn, Previously Presented) A device according to claim 81, wherein said pixel electrode is transparent.

83. (Withdrawn, Previously Presented) A device according to claim 81, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

84. (Withdrawn, Previously Presented) A device according to claim 81, wherein said semiconductor island is a crystalline semiconductor island.

85. (Withdrawn, Previously Presented) A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having anti-ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

86. (Withdrawn, Previously Presented) A television according to claim 85, wherein said pixel electrode is transparent.

87. (Withdrawn, Previously Presented) A television according to claim 85, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

88. (Withdrawn, Previously Presented) A television according to claim 85, wherein said semiconductor island is a crystalline semiconductor island.

89. (Withdrawn, Previously Presented) A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and

a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having anti-ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

90. (Withdrawn, Previously Presented) A portable computer according to claim 89, wherein said pixel electrode is transparent.

91. (Withdrawn, Previously Presented) A portable computer according to claim 89, wherein said thin film transistor is a top-gate type in which said gate electrode is located above said channel region.

92. (Withdrawn, Previously Presented) A portable computer according to claim 89, wherein said semiconductor island is a crystalline semiconductor island.

93. (Withdrawn, Previously Presented) A projector having at least one liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

a second substrate opposed to said first substrate;

at least one thin film transistor being formed over said first substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

wherein said channel region, said source and drain regions of said one thin film transistor is formed in a semiconductor island;

a leveling film formed over said first substrate to provide a leveled upper surface over said first substrate, said leveling film covering said thin film transistor;

a pixel electrode formed on said leveled upper surface, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said leveling film;

a liquid crystal material having anti-ferroelectricity and being formed between said first substrate and said second substrate;

an opposed electrode formed over said second substrate and opposed to said pixel electrode with said liquid crystal material interposed therebetween.

94. (Withdrawn, Previously Presented) A projector according to claim 93, wherein said semiconductor island is a crystalline semiconductor island.

95. (Withdrawn, Previously Presented) A projector according to claim 93, wherein said pixel electrode is transparent.

96. (Withdrawn, Previously Presented) A projector according to claim 66, wherein said leveling film comprises organic resin.

97. (Withdrawn, Previously Presented) A projector according to claim 93, wherein said leveling film comprises organic resin.

APPENDIX B

REFERENCES

Copies attached.

APPENDIX C

EVIDENCE APPENDIX

Not applicable.

APPENDIX D

RELATED PROCCEDINGS APPENDIX

Not applicable.